IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: **Ahrens et al.**

MMB Docket No. **1890-0037**

Application No. **10/755,844**

Filed: **January 12, 2004**

For: **Method for Fabrication of a Contact Structure**

Examiner: **To be assigned**

Group Art Unit: **2812**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

March 3, 2005
(Date of deposit)

James D. Wood
Name of person mailing Document or fee

Signature

March 3, 2005
Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicants hereby disclose the following reference regarding the above-identified patent application. A copy of the foreign documents are enclosed.

Patent References

U.S. Patent No.	Inventor	Issue Date
6,348,731 B1	Ashley et al.	Feb. 19, 2002
5,618,752	Gaul	Apr. 8, 1997
5,608,264	Gaul	Mar. 4, 1997

U.S. Patent Application	Inventor	Publication Date
US 2001/0054769 A1	Raaijmakers et al.	Dec. 27, 2001
US 2002/0163072 A1	Gupta et al.	Nov. 7, 2002
US 2003/0215984 A1	Pogge e5t al.	Nov. 20, 2003

Foreign References	Publication Date	Country Code
WO 03/079431 A	Sept. 25, 2003	WO
EP 1 391 924 A1	Feb. 25, 2004	EP
FR 2 816 758	May 17, 2002	FR
JP 2002/190477	July 5, 2002	JP
EP 1 094 504 A2	April 25, 2001	EP
DE 19816245	Oct. 21, 1999	DE

Articles

1) Burkett et al., "Processing Techniques for 3-D Integration Techniques", Superficies y Vacio 13, 1-6, December 2001, 6 pages.

English translations of the Abstracts for FR 2 816 758 A1, JP 2002190477 and DE 19816245 are enclosed.

EP 1 391 924 A1 corresponds to WO 03/079431 A.

FR 2 816 758 A1 describes an electroplating method wherein interconnections of integrated circuits are formed. A damascene structure is formed on a surface of a substrate whereon a barrier diffusion layer is deposited comprising tungsten. On the barrier diffusion layer, additional layers comprising copper are formed. A layer comprising copper is formed by electroplating and the structure is filled by forming a copper layer.

JP 2002/190477 describes a method for manufacturing a semiconductor device wherein a via hole is formed in a semiconductor substrate. A metal layer is formed on a surface of the via hole and the via hole is filled by electroplating copper. The backside of the substrate is thinned in order to expose the copper material in the via hole. A metal layer for contacting is formed on the backside

Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed within three months after the filing date of the application or before the mailing of the first office action on the merits.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully Submitted,

March 3, 2005

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0037	APPLICATION NO.: 10/755,844
	APPLICANT(S): Ahrens et al.	
	FILING DATE: January 12, 2004	GROUP ART UNIT: 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	6,348,731 B1	Feb. 19, 2002	Ashley et al.			
	AB	5,618,752	Apr. 8, 1997	Gaul			
	AC	5,608,264	Mar. 4, 1997	Gaul			
	AD	2001/0054769 A1	Dec. 27, 2001	Raaijmakers et al.			
	AE	2002/0163072 A1	Nov. 7, 2002	Gupta et al.			
	AF	2003/0215984 A1	Nov. 20, 2003	Pogge et al.			
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	WO 03/079431 A	Sept. 25, 2003	WO			Yes No
	AM	EP 1391924 A1	Feb. 25, 2004	EP			Yes No
	AN	FR 2816758	May 17, 2002	FR			Yes No
	AO	JP 2002190477	July 5, 2002	JP			Yes No
	AP	EP 1094504 A2	Apr. 25, 2001	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ		Burkett et al., "Processing Techniques for 3-D Integration Techniques", Superficies y Vacio 13, 1-6, December 2001. (6 pages).
	AR		
	AS		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0037	APPLICATION NO.: 10/755,844
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	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	DE 19816245	Oct. 21, 1999	DE			Yes No
	AM						Yes No
	AN						Yes No
	AO						Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

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